



RCE 12/07
PATENT
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AUG 29 2002

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Rosengaus et al.

Attorney Docket No.: KLA1P001E1

Application No.: 09/474,941

Examiner: Rosenberger, Richard A.

Filed: December 30, 1999

Group: 2877

Title: SYSTEM AND METHOD FOR
INSPECTING SEMICONDUCTOR WAFERS

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence and the documents and/or fees referred to as attached therein are being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, Washington, DC 20231, or are being facsimile transmitted to the U.S. Patent and Trademark Office, on August 19, 2002.

Signed: *[Signature]*

Tara Hayden

REQUEST FOR CONTINUED EXAMINATION (RCE)
UNDER 37 CFR §1.114

Commissioner for Patents
Box RCE
Washington, DC 20231

This is a Request for Continued Examination (RCE) of the above-identified application.

NOTE: If the above-identified application was filed prior to May 29, 2000, applicant may wish to consider filing a continued prosecution application (CPA) under 37 C.F.R. §1.53(d) instead of an RCE to be eligible for the patent term adjustment provisions of the AIPA.

1. Submission required under 37 C.F.R. §1.114:

- a. Previously submitted
 - i. Consider the amendment/reply under 37 C.F.R. §1.116 previously filed on ____.
(Any unentered amendment referred to above will be entered.)
 - ii. Consider the arguments in the Appeal Brief or Reply Brief previously filed on ____.
 - iii. Other ____.
- b. Enclosed
 - i. Amendment/Reply
 - ii. Affidavit/Declaration
 - iii. Information Disclosure Statement with Form PTO-1449
 Copies of IDS Citations
 - iv. Other ____.

08/28/2002 AWONDAF1 00000076 09474941

01 FC:179
02 FC:115

740.00 OP
110.00 OP

2. **Fees:** (The RCE fee is required at the time the RCE is filed.)

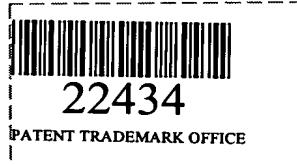
Fee Calculation (37 CFR §1.16)

| | | |
|--|--------------|--------|
| Fee for Request for Continued Examination Under 37 C.F.R. §1.17(e) | \$740 | 740.00 |
| | TOTAL | 740.00 |
| SMALL ENTITY 50% FILING FEE REDUCTION (if applicable) | | |

- a. Applicant hereby petitions for a one month extension of time.
- b. Applicant believes that no (additional) extension of time is required; however, if it is determined that such an extension is required, Applicant hereby petitions that such an extension be granted and authorizes the Director to charge the required fees for an extension of time under 37 CFR §1.136 to Deposit Account No. 500388.
- c. Enclosed is our Check No. 6107 in the amount of \$850.00 to cover the RCE fee, and/or extension of time fees.
- d. The Director is authorized to charge any fees beyond the amount enclosed which may be required, or to credit any overpayment, to Deposit Account No. 500388 (Order No. KLA1P001C1)

3. Please continue to send correspondence to the following address:

Customer Number 022434



Date: 8/19/02


Phillip P. Lee
Registration No. 46,866



PATENT

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I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail to: Assistant Commissioner for Patents, Washington, DC 20231 on August 19, 2002.

Printed Name: Tara Hayden

Signed: 

AMENDMENT E

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

The Examiner is respectfully requested to enter the following amendments and consider the following remarks.

IN THE CLAIMS:

Please CANCEL claims 1, 5-6 and 9, 13-22, and 43-58 without prejudice or disclaimer.

Please ADD claims 59-66 as follows:

59. (Added Claim) A semiconductor manufacturing system comprising:
a wafer handling chamber having a plurality of facets, the wafer handling chamber containing a vacuum environment;
a plurality of wafer processing tools, each of the tools being attached to a respective facet on the wafer handling chamber;
a metrology tool attached to one of the facets of the wafer handling chamber, wherein the metrology tool measures physical parameters on semiconductor wafers; and
a wafer handler located within the wafer handling chamber for transporting wafers between each of the plurality of facets.